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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,537	09/10/2003	Kiyohiko Yamazaki	KAT 253	1951

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EXAMINER	
EJAZ, NAHEED	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,537	YAMAZAKI, KIYOHIKO	
	Examiner	Art Unit	
	Ejaz Naheed	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5/27/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No.2002-342108 filed on 11/26/2002.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 5, 6, 9, 10, 13, 18, 14, and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation "said pulse outputting circuit" on page no.18 lines 4-5. There is insufficient antecedent basis for this limitation in the claim.

Claim 6 recites the limitation "said pulse outputting circuit" on page no.18 lines 10-11. There is insufficient antecedent basis for this limitation in the claim.

Claim 9 recites the limitation "said pulse outputting circuit" on page no.18 lines 29-30. There is insufficient antecedent basis for this limitation in the claim.

Claim 10 recites the limitation "said pulse outputting circuit" on page no.19 lines 7-8. There is insufficient antecedent basis for this limitation in the claim.

Claims 13, 18, 14, and 15 are also rejected because they depend on base rejected claims.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinozaki et al. (US 6,687,512), hereafter referred to as Shinozaki, in view of Hori et al. (US 2003/0117926), hereafter referred to as Hori.

Refer to claim 1, Shinozaki teaches, 'a receiver apparatus comprising: a demodulator for demodulating received radio signals into digital signals (see figure 6, element 162, col.5, lines 58-60); a mode selector for selecting either of a reproduction mode of reproducing the digital signals and an evaluation mode of evaluating the digital signals (see figure 6, element 164, col.6, lines 4-18).

However, Shinozaki fails to disclose an error generator that inverts the digital signal.

Hori teaches, 'an error generator for inverting a level of the digital signals for the evaluation mode at a predetermined timing to generate error data (see figure 2, element 107, page # 4, paragraph # 0052)

It would have been obvious to one of ordinary skill in the art to implement the teaching of Hori into Shinozaki as to distinguish between two types of modes

by the selected inverted signals as taught by Hori (see page # 2, paragraph # 0016).

Refer to claim 2, Shinozaki discloses, 'said mode selector comprises: a first selector (see figure 6, element 164, col.6, lines 4-18); and a second selector (see figure 6, element 168, col.6, lines 4-18)). Furthermore, it would have been obvious to one skilled in the art to incorporate the selectors of Shinozaki to select a destination of digital signals and a source as to be able to switch to different modes based on the types of the signals inputted as taught by Shinozaki (see col.2, lines 15-19).

Refer to claim 3, Shinozaki teaches all the limitations of the claimed invention but he fails to disclose a pulse outputting circuit and an inverter.

Hori teaches, 'said error generator comprises: a pulse outputting circuit for outputting pulse signals at the predetermined timing (see figure 2, element 110, page # 3, paragraph # 0045 and 0047, and page # 4, paragraph # 0054) (Note: element 103 supplies pulse to element 110); and an inverter for inverting the level of the digital signals responsive to a transmission of the pulse signals (see figure 3, element 601, page # 3, paragraph # 0045 and 0046).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Hori into Shinozaki as to detect and set the value of an error signal as taught by Hori (see page # 5, paragraph # 0073).

Refer to claim 4, Shinozaki teaches all the limitations of the claimed invention but he fails to disclose a preset value holding circuit.

Hori discloses, 'said error generator (see figure 2, element 107, page # 4, paragraph # 0052) comprises a preset value holding circuit (see figure 2, element 108, page # 4, col.1, paragraph # 0054) which has a preset value defining a transmission timing of the pulse signals set from outside said apparatus to hold the preset value to supply the preset value to said pulse outputting circuit (see figure 2, element 110, figure 3) and (page # 3, paragraph # 0046 and 0047).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Hori into Shinozaki in order to divide and synchronize and external clock or pulse as taught by Hori (see page # 1, col.2, paragraph # 0013, lines 45-49).

Refer to claim 5, Shinozaki teaches all the limitations of the claimed invention but he fails to disclose an error detector explicitly.

Hori discloses, 'an error detector (see figure 2, element 109A or 109B) interconnected to said mode selector for detecting an error contained in the digital signals (see figure 2, element 102); said error detector supplying said pulse outputting circuit (see figure 2, element 110) with an output timing defining a field of the digital signal in which check data for received data are held' (see page # 3, col.2, paragraph # 0047).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Hori into Shinozaki in order to have signals in synchronization with pulse generator as taught by Hori (see page # 3, col.2, paragraph # 0049, lines 27-30).

Claim 6 is rejected under the same rational as claim 5.

Claim 7 is rejected under the same rational as claim 5.

Claim 8 is rejected under the same rational as claim 5.

Refer to claim 9, Shinozaki teaches all the limitations of the claimed invention but he fails to disclose a sync pattern detector.

Hori discloses, 'a sync pattern detector interconnected to said mode selector for detecting a sync pattern contained in the digital signals (see figure 2, elements 102 and 105); said synchronous pattern detector supplying said pulse outputting circuit with an output timing defining a field of received data which follows the sync pattern and holds check data' (see figure 2, elements 102, 105, and 106, page # 3, col.2, paragraph # 0050 and page # 5, col.2, paragraph # 0070).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Hori into Shinozaki as to detect the fix pattern and output a sync pattern detection as taught by Hori (see page # 2, col.1, paragraph # 0018, lines 17-20).

Claim 10 is rejected under the same rational as claim 9.

Claim 11 is rejected under the same rational as claim 9.

Claim 12 is rejected under the same rational as claim 9.

Claim 13 is rejected under the same rational as claim 9.

Refer to claim 14, Shinozaki teaches all the limitations of the claimed invention but he fails to disclose an error detector and a time selector explicitly.

Hori discloses, 'an error detector for detecting an error contained in the digital signals (see figure 2, elements 109A, and 109B combined, page # 4,

paragraph # 0053 and 0058); and a timing selector for selecting an output timing supplied from either of said error detector and said sync pattern detector' (see figure 2, element 106) and (page # 3, paragraph # 0049 and page # 4, paragraph # 0052).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Hori into Shinozaki in order for a time selector to check if the inputted signal by error detector represents the presence or absence of error signal as taught by Hori (see page # 4, col.1, paragraph # 0052, lines 9-12) and if the inputted sync detection signal represents the absence or presence of the detection to timing generator as taught by Hori (see page # 3, paragraph # 0049, col.2, lines 27-46 and paragraph # 0050).

Claim 15 is rejected under the same rational as claim 14.

Claim 16 is rejected under the same rational as claim 14.

Claim 17 is rejected under the same rational as claim 14.

Claim 18 is rejected under the same rational as claim 14.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The Hagiwara reference, 5,105,426 published on 04/14/1992 "Device For Detecting The Position Of Broken Line In a Series Controller" and The Lee reference, US 6,388,701 published on 05/14/2002, "Device And Method For Removing Co-Channel Interference Signal In Modulation/Demodulation Receiver Having Reference Signal", The Wakabayashi

reference, US 6,643,342, filed on 07/12/1999, "Unique Word Detection Circuit", The Maruyama reference 6,005,896, published on 12/21/1999, "Radio Data Communication Device And Radio Data Communication Method", The Fujiwara et al. reference, US 2001/0020285, filed on 02/22/2001, "Received-Signal Combining Method And System", and the Beck reference, 3,609,507, filed on 05/05/1970, "Polyphase Inverter System Having Fault Protection And Output Amplitude Regulation Through Pulse Width Modulation".

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naheed Ejaz whose telephone number is 571-272-5947. The examiner can normally be reached on Monday - Friday 8:00 - 4:30.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Naheed Ejaz
Examiner
Art Unit 2631

6/7/2005

EMMANUEL BAYARD
PRIMARY EXAMINER